

The Implementation of 8051 MCU for IC-EMC Testing

Mao-Hsu Yen*, Yih-Hsia Lin**, Yin-Cheng Chang*** & Pei-Jung Tsai****

*Computer Science and Engineering, National Taiwan Ocean University, Keelung, TAIWAN, ROC.

E-Mail: ymh{at}email{dot}ntou{dot}edu{dot}tw

**Department of Electronic Engineering, Ming Chuan University, Taoyuan, TAIWAN, ROC.

E-Mail: yslin{at}mail{dot}mcu{dot}edu{dot}tw

***National Chip Implementation Center, National Applied Research Laboratories, Hsinchu, TAIWAN, ROC.

E-Mail: yincheng.chang{at}narlabs{dot}org{dot}tw

****Computer Science and Engineering, National Taiwan Ocean University, Keelung, TAIWAN, ROC.

E-Mail: b09902067{at}gmail{dot}com

Abstract—In recent years, several new methods for IC-level electromagnetic compatibility (EMC) testing have been introduced. Therefore, a handy vehicle for IC-EMC test is required to validate the effectiveness of the new IC-EMC testing methods. The ease-of-use, wide applicability, and high reliability of 8051 microcontroller units (MCUs) has led to their wide-scale application in embedded systems. To extend the scope of the application of 8051 MCU, this study implements an 8051 MCU of MC8051 architecture with I²C bus interface as a vehicle for EMC testing. The advantage of I²C is its ability of in-system programming (ISP), which allows the firmware upgrades of 8051 with a personal computer using an inexpensive download cable and therefore provides enhanced flexibility of 8051 for EMC testing. An IC-EMC testing platform composed of a multifunction test board and several off-board probes was fabricated according to IEC 61967 and IEC 62132 standards. It demonstrates the method to use the proposed 8051 chip in EMC testing and reveals the results of its EMC performance.

Keywords—8051; Electromagnetic Compatibility; Electromagnetic Compatibility of Integrated Circuits; In-System Programming; Microcontroller.

Abbreviations—Electromagnetic Compatibility (EMC); In-System Programming (ISP); Microcontroller (MCU).

I. INTRODUCTION

THE 8051 is an 8-bit microprocessor originally designed in the 1980s by Intel. Its standard form is a single-chip implementation that includes several useful on-chip peripherals, including timers, interrupt, counters, and UARTs, as well as 4K bytes of on-chip program memory and 128 bytes of data memory. Many companies have manufactured derivatives of the 8051 with additional on-chip peripherals, such as analog-digital converters, pulse-width modulators, and the Philips I²C bus [Philips Semiconductor, 2] interfaces. The interface between microprocessors (serial and parallel) and peripheral devices is crucial to the exchange of data. Parallel connections use a greater number of lines for high-speed transmission, which is suitable only for short distances. Serial connections have fewer lines and a simpler structure, which operate at slow speeds over long distances. In particular, the high-performance synchronous serial bus of the I²C is able to communicate with multi-host systems and synchronize high-

and low-speed devices. The ease-of-use and flexibility of the interface has led to its wide-spread implementation in circuit design.

I²C can be used to control various types of IC using two lines to achieve full-duplex synchronous transmission for multi-host systems with a variety of peripheral devices. We want to add an I²C (Inter-Integrated Circuit) [Jai Karan Singh et al., 11] function because MC8051 [Oregano Systems, 13] lacks a control interface. The addition of I²C functionality enables the 8051 chip to communicate with peripheral devices that also feature an I²C interface, thereby improving expansion capabilities of the 8051. In this paper, we applied cell-based design flow to equip the 8051 MCU [Mussolini, 12] with I²C functionality and an embedded SRAM IP (Intellectual Property). All of them were realized with TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μ m technology served by the National Chip Implementation Center (CIC).

In the following section, we describe the architecture of the proposed MC8051 with I²C bus interface. In Section 3, we illustrate how the I²C IP core was combined with the MC8051 and describe the implementation of the Electromagnetic compatibility (EMC) testing PCB. Several different IC-EMC measurements complied with IEC standards can be performed on the same board by careful design and the pre-reserved test points with certified off-board probes. Conclusions are drawn in Section 4.

II. ARCHITECTURE AND SYSTEM ANALYSIS OF 8051 WITH I²C

This study developed a new 8051 MCU comprising an MC8051 core, I²C interface, and in-system programming (ISP) [Bonnett, 1] mechanism for an IC-EMC testing platform (Figure 1). The open source IP core of the MC8051 was developed by Oregano Systems and the Vienna

University of Technology [Oregano Systems, 13]. The architecture is based on the Intel 8051 and uses VHDL to ensure that the instruction set is compatible with the standard Intel 8051. The MC8051 microcontroller consists of a microprocessor and a variety of peripherals, including timers, general purpose IO (GPIO), communications interfaces, and memory (ROM and/or RAM).

Table 1 lists the ISP mechanism and control signals of the 8051 MCU. In the proposed 8051 MCU, the main object copies the “program rom” (hex file) to SRAM (TSMC Artisan Memory Generator). TSMC SRAM provides advantages in area overhead and speed capable of improving the overall performance of the 8051. The proposed MCU includes four ports, each of which has eight input/output lines, resulting in a total of 32 I/O lines. All 32 of the I/O pins of the microcontroller are configured as input/output pins. Table 2 lists the signals between the 8051 MCU and I²C, which is used for the attachment of lower speed peripherals.

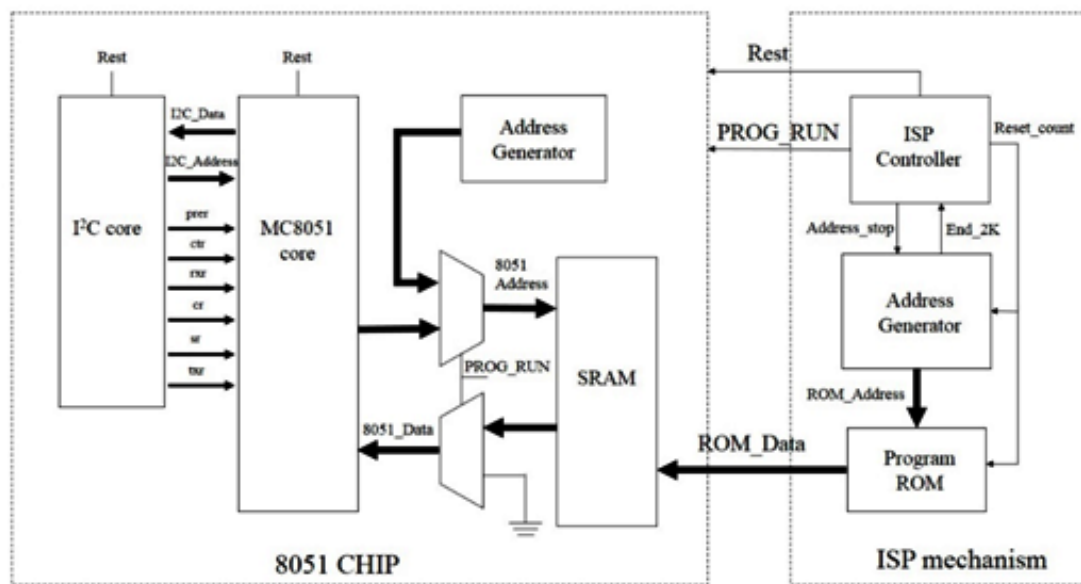


Figure 1: Block Diagram of Proposed 8051 MCU with I²C

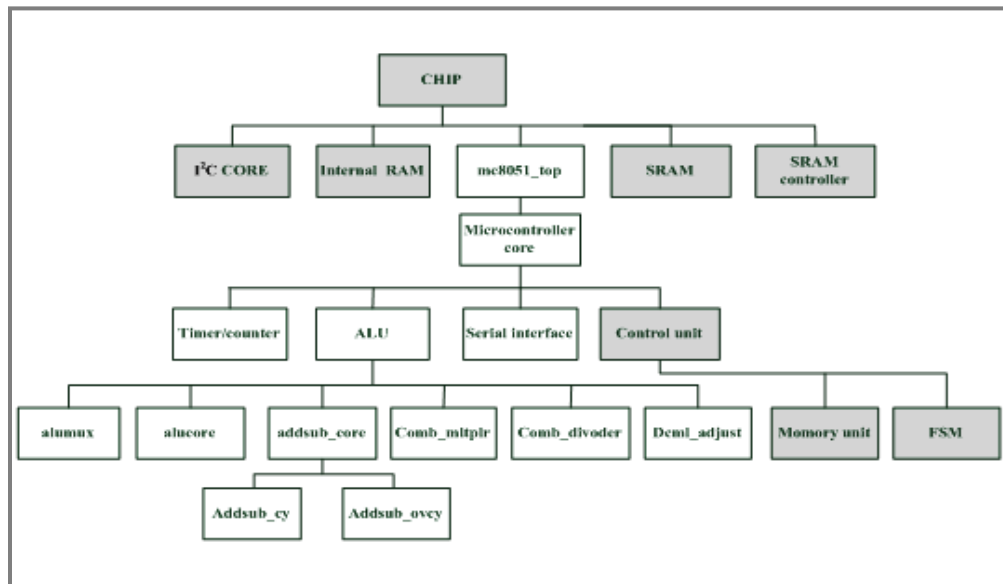
Table 1: Signals of 8051 MCU and ISP Mechanism

Signals	Function
Reset_count	Reset SRAM controller
PROG_RUN	Switch PROG or RUN mode
End_2K	Notify the counting address up to 2K
Address_stop	Stop Controller Address Generator
ROM_Address	Address input of Program ROM
ROM_data	Data output of Program ROM
8051_Address	address output of 8051
8051_data	data input of 8051
Rest	Reset 8051

Table 2: Signals between 8051 MCU and I²C

Signals	Function
prer	Clock Prescale Register output
ctr	Control Register output
rxr	Receive Register output
cr	Command Register output
sr	Status Register output
txr	Transmit Register output
I2C_Address	Input I ² C address
I2C_data	Input I ² C data

Figure 2 presents a hierarchy chart for the MC8051 with I²C in which the white cells are original MC8051 modules and grey cells have been changed. We also added an interrupt to the I²C and a controller for writing and reading to the SRAM. Internal RAM (128 bytes) substitutes for Artisan Memory Generator’s 0.18 um register file, and ROM substitutes for 0.18 um SRAM (2K bytes) which is also generated by Artisan Memory Generator.

Figure 2: Hierarchical Design of MC8051 with I²C

2.1. ISP Controller

The main function of the ISP controller is to control the reading, writing, and execution of data by the MC8051. The ISP control module in this study was designed using the finite state machine, including the four states shown in Figure 3.

- **START0**
When the reset signal is sent, the ISP controller enters the initial state referred to as 'START0'. In this state, the 8051 and "address generator" are reset, whereupon the SRAM in 8051 enter the programming state.
- **START1:**
The system is maintained in reset mode for a period sufficient to ensure that the system is stable as START0.
- **PROGRAM:**
The program burns 2K bytes of data to the SRAM and then enters RUN state after the SRAM controller receives the End_2K signal.
- **RUN:**
The controller enters the execution state in which the 8051 begins data execution in SRAM. It remains in this state until it receives a reset signal.

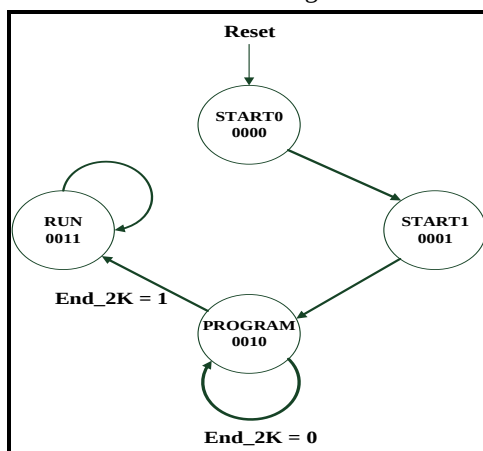


Figure 3: State Diagram of ISP Controller

2.2. Architecture of I²C Interrupt

As shown in Table 3, the proposed 8051 includes five interrupts: two external (int0, int1), two timer/counter interrupts (TF0, TF1), and one serial port interrupt (TXD, RXD).

Table 3: 8051 Interrupt Vector

Interrupt Number	Function Vector	Flag	Function Description
-	0x00	-	System reset (Reset)
0	0x03	IE0	External interrupt (INT0)
1	0x0B	TF0	Timer/Counter interrupt (TF0)
2	0x13	IE1	External interrupt (INT1)
3	0x1B	TF1	Timer/Counter interrupt (TF1)
4	0x23	TI, RI	Serial port interrupt (TXD, RXD)

The Interrupt Enable Register (IER) can be regarded as a switch for the exchange of interrupt functions used to determine the priority of each interrupt in accordance with the Interrupt Priority Register (IPR).

We also used the 6th reserved bit to define EI2C and PI2C respectively in IE and IP adding the dedicated interrupt of I²C like Table 4 and Table 5 and the interrupt vector address of I²C using 33H as shown in Table 6. First, initiating the I²C interrupt function requires that the 6th and 7th bits be set in IE. Second, we enter the interrupt vector of I²C to obtain the address of the interrupt for the execution of the interrupt function.

Table 4: Interrupt Enable Register

IER addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8H	EA	EI2C	ET2	ES	ET1	EX1	ET0	EX0

Table 5: Interrupt Priority Register

IPR addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8H	-	PI2C	PT2	PS	PT1	PX1	PT0	PX0

Table 6: I²C Interrupt Vector

Interrupt name	Interrupt Vector	Flag	Function Description
I ² C	0033H	EI2C	I ² C interrupt

III. IMPLEMENTATION

In this paper, we employed cell-based design flow to complete the design of the 8051 MCU chip [Mao-Hsu Yen, 14]. The synthesis of the chip was achieved using Synopsys design compiler and the layout was completed using SOC Encounter, as shown in Figure 4. The finished chip covers an area of 1.2 mm × 1.2 mm with 86 IO pins, and has an internal core operating at 1.8V, an external IO PAD using 3.3V, and a maximum frequency of 110 Mhz. These specifications are listed in Table 7.

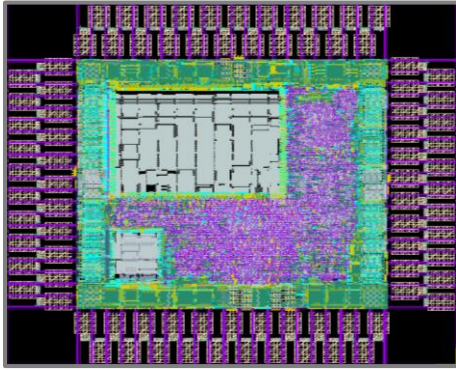


Figure 4: Layout of 8051 MCU

Table 7: Specifications of 8051

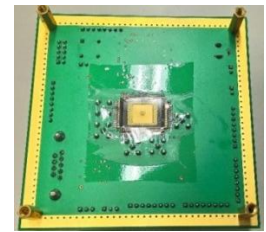
Items	Total
Technology	TSMC 0.18 um
Area	1.2 mm × 1.2 mm
I/O Pads	86 pins
Package	CQFP100
Core Voltage	1.8V
Pad Voltage	3.3V
Speed	110 Mhz

As shown in Figure 5, the 8051 MCU chip and IC-EMC testing platform [Mao-Hsu Yen, 16] composed of a multifunction test board with several off-board probes were manufactured in accordance with IEC 61967 [3; Ostermann, 5] and IEC 62132 [7] standards. To guarantee the meaningful EMC results measured from the test board, basic design recommendation described in the standard should be followed. For example, this board used the stackup with a 1.6mm thick four-layer board including a ground layer, power supply layer, signal layer, and a ground or signal layer. And all of the elements, such as the power connector and signal connector, are soldered on the same side with the measured wafer placed on the other side. Considering the capability of performing several tests via the same multifunction test board, extra critical principles should be

noted. The location of these EMC test points should be reserved preferentially and is desired to be put as close as possible to the pin under test to reduce parasitic. Besides, this work aggressively combined six methods on a test board. The approach is to build the probes and networks needed in these standards to be off-board type. These off-board probes as shown in Figure 6 can be used repeatedly with certified characteristics [Yin-Cheng Chang, 17]. This solution not only saves the cost without building these probes on the various one-time-use test boards, but also keeps the measured results highly repeatable and reproducible because each of them can be verified carefully before experiment. The most important part in this board design is the partition between local ground under IC and the global ground which is especially designed for 1Ω direct coupling method [Yin-Cheng Chang, 15]. When other test method is preceded, a short termination is used to connect the local ground and global ground together. Figure 7 shows possible cases of the test setup to demonstrate the practical experiments with different methods. Figure 8 shows the measured emission by using the 150Ω method [IEC 61967-4, 8] while the designated I/O port output a signal of 6 kHz clock rate. The result can be used to estimate the conducted emission level from the MCU. For immunity evaluation, Figure 9 shows the measured waveform at an I/O port to monitor the noise variation while the RF interference is injected through the DPI probe. With measured data from various methods could help to analyse and model the MCU.

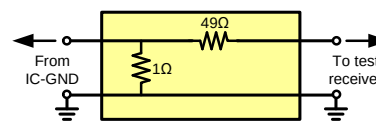


(a) Front Side

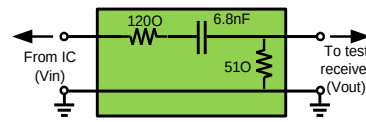


(b) Back side

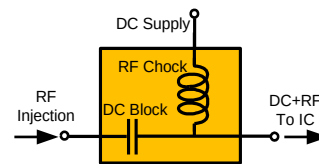
Figure 5: Testing Board and 8051 MCU for IC-EMC



(a)



(b)



(c)

Figure 6: (a) The 1Ω current probe; (b) the 150Ω voltage probe; (c) the DPI [IEC 62132-4, 9] probe

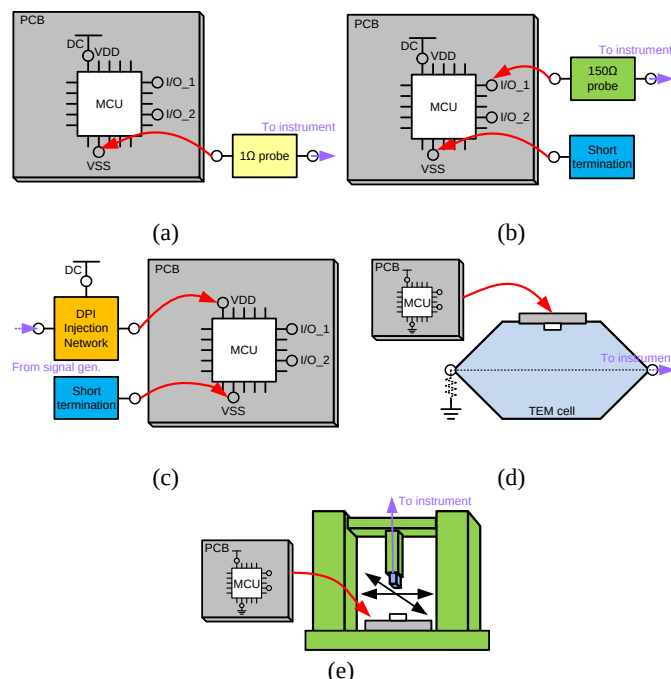


Figure 7: The test setups for IC-EMC evaluation based on the multifunction test board: (a) 1Ω method for conducted emission, (b) 150Ω method for conducted emission, (c) DPI method for conducted immunity, (d) TEM cell method [IEC 61967-2, 6; IEC 62132-2, 10] for both radiated emission and immunity, and (e) near field scan method [IEC 61967-6, 4] for radiated emission

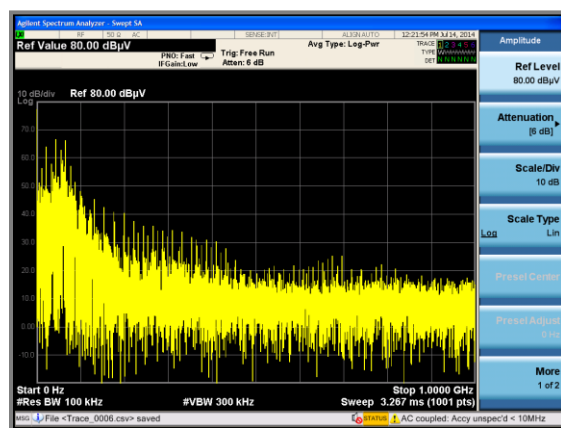


Figure 8: The Measured Emission Spectrum by using the 150Ω Probe

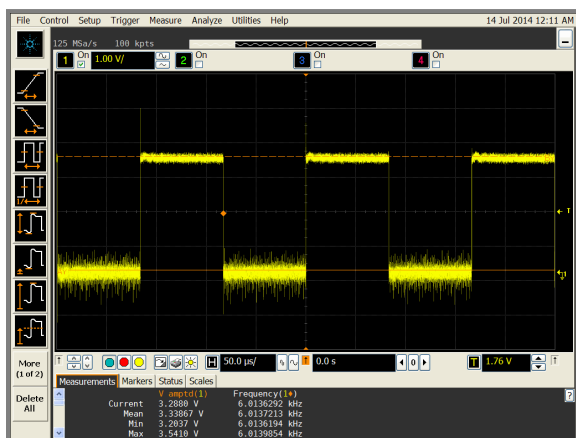


Figure 9: The Measured Waveform while Applying DPI Method

IV. CONCLUSION

This paper proposes a new 8051 MCU chip with ISP and I²C based on the MC8051 architecture fabricated using TSMC 0.18 μm CMOS technology. The 8051 MCU is reprogrammable using existing devices, such as a PC via an inexpensive interface and is fully compatible with the Intel 8051 microcontroller. A PCB testing board with ISP for investigating IC-EMC was fabricated in accordance with IEC 61967 and IEC 62132 standards. We show that the method to use the 8051 chip with ISP in EMC testing and reveal the results of its EMC performance.

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Mao-Hsu Yen received the B.S., M.S., and Ph.D. degrees in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1991, 1993, and 2000, respectively. Department of Computer Science and Engineering, National Taiwan Ocean University, Keelung, Taiwan, since 2005, where he is currently an Associate Professor. His current research

interests include the design of application-specific integrated circuit, MCU and FPGA architectures.



Yih-Hsia Lin received the Ph.D. degree in Electronics Engineering from National Chiao Tung University of Taiwan, R.O.C., in 2001. Since August 2003, she has been with the Department of Electronics Engineering, Ming Chuan University, where she was an Assistant Professor, became an Associate Professor in 2010.



Yin-Cheng Chang received the M.S. degree from Feng-Chia University, Taichung, Taiwan, in 2005, and he is currently working toward the Ph.D. degree at the institute of electronics, National Tsing Hua University, Hsinchu, Taiwan. In 2005, he joined the National Chip Implementation Center, Hsinchu, Taiwan, where he was responsible for high frequency measurement technology

development and service until 2010. Since 2011, he was involved with system in package (SiP) group as an associate researcher. His research interests include RF/MW circuits design measurement, SI/PI, and IC-EMC, with over 30 technical publications and patents. He is a member of Phi Tau Phi.



Pei-Jung Tsai received the B.S. degree from Chung-Hua University, Hsinchu, Taiwan, in 2014, and she is currently working toward the M.S. degree at the Department of Computer Science and Engineering, National Taiwan Ocean University, Keelung, Taiwan. She current research interests include the design of VLSI Design and MCU architectures.